The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (cancelled)

Claim 2 (new): A semiconductor device comprising:

a memory cell array having NAND cells arranged therein;

a plurality of latch circuits which temporarily hold data read out from said memory cell array;

a first circuit configured to generate a first current varying in proportion to "1" or "0" of binary logic data of one end of said plurality of latch circuits;

a second circuit configured to generate a second current which is preset; and

a third circuit configured to compare the first current with the second current;

wherein the value of "1" or "0" of binary logic data of said one end of said plurality of latch circuits is detected based on a result of the comparison between the first current and the second current.

Claim 3 (new): The semiconductor device according to claim 2, wherein an output current of said second circuit is variable and can be set to vary in the same steps as the steps in which the first current varies.

Claim 4 (new): The semiconductor device according to claim 2, wherein the minimum value of the second current is larger than the minimum value of the first current and the maximum value of the second current is smaller than the maximum value of the first current.

Claim 5 (new): The semiconductor device according to claim 2, wherein said third circuit includes a first MOS transistor which is diode-connected to cause the first current to flow there through, and a second MOS transistor having a gate potential equal to a gate potential of said first MOS transistor and having a drain connected to said second circuit.

Claim 6 (new): The semiconductor device according to claim 2, wherein data read out from said memory cell array is data obtained after a verify readout is performed in one of a program operation and erase operation.

Claim 7 (new): The semiconductor device according to claim 2, wherein the value of "1" or "0" detected from said one end of said plurality of latch circuits is equal to the number of failed bits after a verify readout of a program operation is performed.

Claim 8 (new): The semiconductor device according to claim 2, wherein

said first circuit includes a plurality of current passage circuits connected in parallel, each including a first MOS transistor having a gate applied with a preset fixed potential, a second MOS transistor having a current path serially connected to a current path of said first MOS transistor and having a gate potential directly or indirectly controlled based on a potential of said one end of said plurality of latch circuits and a first switching element connected in series with the current paths of said first and second MOS transistors; and

said second circuit includes a plurality of current passage circuits each including a third MOS transistor which is the same size as said first MOS transistor and having a gate applied with the fixed potential, a fourth MOS transistor having a current path serially connected to a current path of said third MOS transistor and having a gate controlled by a control signal used for setting a second current value and a second switching element connected in series with the current paths of said third and fourth MOS transistors, and a current passage circuit configured to generate a current smaller than the current which has a value smaller than that of one of the plurality of current passage circuits of said first circuit.

Claim 9 (new): The semiconductor device according to claim 8, wherein said first and second switching elements include fuse elements.

Claim 10 (new): The semiconductor device according to claim 8, wherein said first and second switching elements include MOS transistors having gates which are controlled.

Claim 11 (new): A semiconductor device comprising:

a memory cell array having NAND cells arranged therein;

a plurality of latch circuits which temporarily hold data to be programmed into said memory cell array;

a first circuit configured to generate a first current varying in proportion to "1" or "0" of binary logic data of one end of said plurality of latch circuits;

a second circuit is configured to generate a second current which is preset; and

a third circuit configured to compare the first current with the second current;

wherein the value of "1" or "0" of binary logic data of said one end of said plurality of latch circuits is detected based on a result of the comparison between the first current and the second current.

Claim 12 (new): The semiconductor device according to claim 11, wherein an output current of said second circuit is variable and can be set to vary in the same steps as the steps in which the first current varies.

Claim 13 (new): The semiconductor device according to claim 11, wherein the minimum value of the second current is larger than the minimum value of the first current and the maximum value of the second current is smaller than the maximum value of the first current.

Claim 14 (new): The semiconductor device according to claim 11, wherein said third circuit includes a first MOS transistor which is diode-connected to cause a first current to flow there through, and a second MOS transistor whose gate potential is equal to that of said first MOS transistor and whose drain is connected to said second circuit.

Claim 15 (new): The semiconductor device according to claim 11, wherein the value of "1" or "0" detected from said one end of said plurality of latch circuits is equal to the number of program data items accompanied by a shift in a threshold voltage in a program operation.

Claim 16 (new): The semiconductor device according to claim 11, wherein

said first circuit includes a plurality of current passage circuits connected in parallel, each including a first MOS transistor having a gate applied with a preset fixed potential, a second

MOS transistor having a current path serially connected to a current path of said first MOS transistor and having a gate potential directly or indirectly controlled based on a potential of said one end of said plurality of latch circuits, and a first switching element connected in series with the current paths of said first and second MOS transistors; and

said second circuit includes a plurality of current passage circuits each including a third MOS transistor which is the same size as said first MOS transistor and having a gate applied with the fixed potential, a fourth MOS transistor having a current path serially connected to a current path of said third MOS transistor and having a gate controlled by a control signal used for setting a second current value and a second switching element connected in series with the current paths of said third and fourth MOS transistors, and a current passage circuit configured to generate a current which has a value smaller than that of one of the plurality of current passage circuits of said first circuit.

Claim 17 (new): The semiconductor device according to claim 16, wherein said first and second switching elements include fuse elements.

Claim 18 (new): The semiconductor device according to claim 16, wherein said first and second switching elements include MOS transistors having gates which are controlled.

Claim 19 (new): A semiconductor device comprising:

a memory cell array having NAND cells arranged therein;

a plurality of latch circuit groups each including a preset number of latch circuits which temporarily hold data read out from said memory cell array;

a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit group of the plurality of the latch circuit groups when binary logic data of one end of said plurality of latch circuit groups is "0", and interrupt the current when the binary logic data is "1", said first circuit outputting a first current which is a sum of currents flowing through the current path;

a second circuit configured to generate a second current which is preset; and

a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of binary logic data of said one end of the plurality of latch circuit groups based on a result of the comparison between the first current and the second current.

Claim 20 (new): The semiconductor device according to claim 19, wherein said plurality of latch circuit groups each include at least a sense amplifier or a data register simultaneously selected by a column address.

Claim 21 (new): The semiconductor device according to claim 19, wherein the value of "1" or "0" detected from said one end of said plurality of latch circuit groups is equal to the number of failed bytes after a verify readout of a program operation is performed.

Claim 22 (new): The semiconductor device according to claim 19, wherein an output current of said second circuit is variable and can be set to vary at the same interval as an interval at which the first current varies.

Claim 23 (new): The semiconductor device according to claim 19, wherein the minimum value of the second current is larger than the minimum value of the first current and the maximum value of the second current is smaller than the maximum value of the first current.

Claim 24 (new): The semiconductor device according to claim 19, wherein said third circuit includes a first MOS transistor which is diode-connected to cause a first current to flow there though, and a second MOS transistor having a gate potential equal to a gate potential of said first MOS transistor and having a drain connected to said second circuit.

Claim 25 (new): The semiconductor device according to claim 19, wherein

said first circuit includes a plurality of current passage circuits connected in parallel, each including a first MOS transistor having a gate applied with a preset fixed potential, a second MOS transistor having a current path serially connected to a current path of said first MOS transistor and having a gate potential directly or indirectly controlled based on a potential of said

one end of said plurality of latch circuits and a first switching element connected in series with the current paths of said first and second MOS transistors; and

said second circuit includes a plurality of current passage circuits each including a third MOS transistor which is the same size as said first MOS transistor and having a gate applied with the fixed potential, a fourth MOS transistor having a current path serially connected to a current path of said third MOS transistor and having a gate controlled by a control signal used for setting a second current value and a second switching element connected in series with the current paths of said third and fourth MOS transistors, and a current passage circuit which generates a current which has a value smaller than that of one of the plurality of current passage circuits of said first circuit.

Claim 26 (new): The semiconductor device according to claim 25, wherein said first and second switching elements include fuse elements.

Claim 27 (new): The semiconductor device according to claim 25, wherein said first and second switching elements include MOS transistors having gates which are controlled.

Claim 28 (new): The semiconductor device according to claim 19, wherein data read out from said memory cell array is data obtained after a verify readout is performed in one of a program operation and erase operation.

Claim 29 (new): The semiconductor device according to claim 28, wherein a basic unit which is replaced by a redundancy column circuit includes one of said latch circuit groups.

Claim 30 (new): The semiconductor device according to claim 19, wherein said first circuit includes a switch configured to separate a defective current path.

Claim 31 (new): The semiconductor device according to claim 30, wherein said switch includes a fuse element.

Claim 32 (new): The semiconductor device according to claim 30, wherein said switch includes a MOS transistor having a gate which is controlled.

Claim 33 (new): A semiconductor device comprising:

a memory cell array including NAND cells arranged therein;

a plurality of latch circuits which temporally hold data read out from the memory cell array;

a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit of the plurality of the latch circuits when binary logic data of one end of said plurality of latch circuits is "0", and interrupt the current when the binary logic data is "1", said first circuit outputting a first current which is a sum of currents flowing through the current path;

a second circuit configured to generate a second current which is predetermined;

a current control circuit connected to the first and second circuits, and configured to determine absolute values of the first current and the second current; and

a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of the binary logic data of said one end of the plurality of latch circuits based on a result of the comparison between the first current and the second current.

Claim 34 (new): The semiconductor device according to claim 33, wherein a signal for controlling the second current is input to the second circuit, and the second current varies in units of the same value as the first current.

Claim 35 (new): The semiconductor device according to claim 33, wherein:

the first circuit comprises a plurality of current paths each of which includes (i) a first transistor having a gate voltage directly or indirectly controlled by the binary logic data of the one end of the plurality of latch circuits, (ii) a second transistor to which an output signal of the current control circuit is to be input, and (iii) a fuse element; and

the second circuit comprises a plurality of second current paths and a third current path, each of the second current paths including (i) a third transistor having a gate to which a second control signal for controlling the second current is to be input, and (ii) a fourth transistor to

which the output signal of the current control circuit is to be input, the third current path allowing current to flow there through, which has a value smaller than a value in units of the first current flowing through the first circuit.

Claim 36 (new): A semiconductor device comprising:

a memory cell array including NAND cells arranged therein;

a plurality of latch circuits which temporarily hold data to be written into the memory cell array;

a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit of the plurality of the latch circuits when binary logic data of one end of said plurality of latch circuits is "0", and interrupt the current when the binary logic data is "1", said first circuit outputting a first current which is a sum of currents flowing through the current path;

a second circuit configured to generate a second current which is predetermined;

a current control circuit connected to the first and second circuits, and configured to determine absolute values of the first current and the second current; and

a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of the binary logic data of said one end of the plurality of latch circuits based on a result of the comparison between the first current and the second current.

Claim 37 (new): The semiconductor device according to claim 36, wherein a signal for controlling the second current is input to the second circuit, and the second current varies in units of the same value as the first current.

Claim 38 (new): The semiconductor device according to claim 37, wherein:

the first circuit comprises a plurality of current paths each of which includes (i) a first transistor having a gate voltage directly or indirectly controlled by the binary logic data of the one end of the plurality of latch circuits, (ii) a second transistor to which an output signal of the current control circuit is to be input, and (iii) a fuse element; and

the second circuit comprises a plurality of second current paths and a third current path, each of the second current paths including (i) a third transistor having a gate to which a second control signal for controlling the second current is to be input, and (ii) a fourth transistor to which the output signal of the current control circuit is to be input, the third current path allowing current to flow there through, which has a value smaller than a value in units of the first current flowing through the first circuit.

Claim 39 (new): A semiconductor device comprising:

a memory cell array including NAND cells arranged therein;

a plurality of latch circuit groups each having a predetermined number of latch circuits which temporarily hold data read out from the memory cell array or data to be written into the memory cell;

a first circuit configured to cause a current to flow through a current path connected to a corresponding latch circuit group of the plurality of the latch circuit groups when binary logic data of one end of said plurality of latch circuit groups is "0", and interrupt the current when the binary logic data is "1", said first circuit outputting a first current which is a sum of currents flowing through the current path;

a second circuit configured to generate a second current which is predetermined;

a current control circuit connected to the first and second circuits, and configured to determine absolute values of the first current and the second current; and

a third circuit configured to compare the first current output from the first circuit with the second current output from the second circuit, said third circuit detecting the value of "1" or "0" of the binary logic data of said one end of the plurality of latch circuit groups based on a result of the comparison between the first current and the second current.

Claim 40 (new): The semiconductor device according to claim 39, wherein said plurality of latch circuit groups include at least a sense amplifier or a data register simultaneously selected by one column address.

Claim 41 (new): The semiconductor device according to claim 39, wherein the value of "1" or "0" detected from said one end of said plurality of latch circuit groups is equal to the number of failed bytes after a verify readout of the program operation is performed.

Claim 42 (new): The semiconductor device according to claim 39, wherein a signal for controlling the second current is input to the second circuit, and the second current varies in units of the same value as the first current.

Claim 43 (new): The semiconductor device according to claim 42, wherein:

the first circuit comprises a plurality of current paths each of which includes (i) a first transistor having a gate voltage directly or indirectly controlled by the binary logic data of the one end of the plurality of latch circuits, (ii) a second transistor to which an output signal of the current control circuit is to be input, and (iii) a fuse element; and

the second circuit comprises a plurality of second current paths and a third current path, each of the second current paths including (i) a third transistor having a gate to which a second control signal for controlling the second current is to be input, and (ii) a fourth transistor to which the output signal of the current control circuit is to be input, the third current path allowing a current to flow there through, which has a value smaller than a value in units of the first current flowing through the first circuit.

Claim 44 (new): The semiconductor device according to claim 33, wherein the current control circuit includes a current generator which generates a predetermined current, and applies respective predetermined voltages to the first and second circuits, causing a current varying in proportion to the current generated from the current generator to flow through the first and second circuits.

Claim 45 (new): The semiconductor device according to claim 36, wherein the current control circuit includes a current generator which generates a predetermined current, and applies respective predetermined voltages to the first and second circuits, causing a current varying in

proportion to the current generated from the current generator to flow through the first and second circuits.

Claim 46 (new): The semiconductor device according to claim 39, wherein the current control circuit includes a current generator which generates a predetermined current, and applies respective predetermined voltages to the first and second circuits, causing a current varying in proportion to the current generated from the current generator to flow through the first and second circuits.